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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
DUONG, THOI V

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 07/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,647	JUN, SAHNG-IK	
	Examiner	Art Unit	
	Thoi V Duong	2871	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☒ Claim(s) *25-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 22 and 27 are objected to because of the following informalities: In claim 22, line 9, "forming a on the gate insulating layer light interception pattern" should be --forming on the gate insulating layer a light interception pattern--; and in claim 27, line 11, "from" should be --form--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8, 10-18, and 20-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsueda (USPN 5,247,289).

As shown in Figs. 6 and 7, Matsueda discloses a thin film transistor (TFT) array substrate for a liquid crystal display, the thin film transistor array substrate comprising:

an insulating substrate 71 (Fig. 7);

a plurality of gate lines 62 (Fig. 6) formed on the transparent insulating substrate; and gate electrodes 76 (Fig. 7) connected to the gate lines;

common electrodes 67 (Fig. 6) or 81 (Fig. 7) formed on the substrate at the pixel regions and separated from said gate lines;

a gate insulating layer 80 (Fig. 7) covering said gate lines and said common electrodes;

a semiconductor pattern 78 (Fig. 7) formed on the gate insulating layer over the gate electrodes and made of silicon or compound (col. 6, lines 29-31) which absorbs light;

a light interception pattern formed on the gate insulating layer over the common electrode (on the right side of Fig. 7) and made of same material as the semiconductor pattern;

a plurality of data lines 61 (Fig. 6) comprising a source electrode 77 and a drain electrode 79 (Fig. 7) formed on the semiconductor pattern, and data lines connected to the source electrode and crossing over the gate lines to define a pixel region;

an ohmic contact pattern 88 interposed between the semiconductor pattern and the data line assembly and having the same shape as the data lines; and

pixel electrodes 69 (Fig. 6) or 82 (Fig. 7) formed at the pixel region and spaced apart from the common electrodes with a predetermined distance, wherein the pixel electrode is coupled to the drain electrode;

wherein the light interception pattern is overlapped with the corresponding data line, and the common electrode,

wherein the semiconductor pattern is connected to the corresponding light interception pattern,

wherein the semiconductor pattern is extended to the bottom of the corresponding data line,

wherein the light interception pattern is extended external to the periphery of the corresponding data line,

wherein the common electrodes are formed at the same plane as the gate lines,

wherein the pixel electrodes are formed at the same plane as the data lines,

wherein the semiconductor patterns are extended to the bottom of the pixel electrodes.

Finally, with respect to claim 24, the method of photolithography using a photoresist pattern employed to form the light interception pattern, the semiconductor pattern, the data line assembly and the pixel electrode are well-known in the art.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsueda in view of Ono et al. (USPN 6,377,323 B1).

Matsueda discloses a TFT array substrate that is basically the same as that recited in claims 9 and 19 except that the pixel electrodes are formed at the same plane as the data lines. As shown in Fig. 3, Ono discloses a TFT array substrate comprising a protective layer PSV1 covering a data line assembly DL and having contact holes CN, wherein a pixel electrode ITO1 is formed on the protective layer and connected to a drain electrode through the contact holes. Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the TFT array substrate of Matsueda of with the teaching of Ono by forming the pixel electrode

on the protective layer through holes contacting the drain electrodes so as to obtain a stronger electric field.

Allowable Subject Matter

6. Claims 25-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (703) 308-3171. The examiner can normally be reached on Monday-Friday from 8:00 am to 4:30 pm.

Thoi Duong

07/23/2002

William L. Sikes
Supervisory Patent Examiner
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